AMENDED CLAIM SET:

1. (currently amended) A DRAM, comprising:

at least one primary sense amplifier, wherein the at least one primary sense amplifier has at least two amplification stages, has single ended sensing, has data storage and data write-back capability, wherein the write-back comprises at least one passtransistor;

a plurality of storage cells and a plurality of bitlines, with a single ended bitline structure, wherein one storage cell of the plurality of storage cells and the at least one primary sense amplifier are connected by one single bitline of the plurality of bitlines; and

a plurality of secondary sense amplifiers and a plurality of global bitlines, with a single ended global bitline structure, wherein the at least one primary sense amplifier and one secondary sense amplifier of the plurality of secondary sense amplifiers are connected by one single global bitline of the plurality of global bitlines.

2. (canceled)

3. (currently amended) The DRAM of claim ~~2~~ 1, wherein the DRAM further comprises a small voltage swing design.

4. (currently amended) The DRAM of claim ~~2~~ 1, wherein at least one of the plurality of secondary sense amplifiers comprise at least two amplification stages.

5. (currently amended) The DRAM of claim ~~2~~ 1, wherein the at least one primary sense amplifier is being capable to decouple from the one single global bitline.

6. (original) The DRAM of claim 1, wherein the at least one primary sense amplifier comprises MOS devices, and wherein at least one of the MOS devices has a customized threshold.

7. (original) The DRAM of claim 6, wherein the customized threshold is dynamically adjusted.

8. (original) The DRAM of claim 1, wherein the DRAM is an embedded DRAM.

9. - 23. (canceled)

24. (new) The DRAM of claim 1, wherein the at least one primary sense amplifier further comprises a write capability from the one single global bitline to the one storage cell, wherein the write comprises the at least one passtransistor.